

Understanding the Origin of Thermal Annealing Effects in Low-Temperature Amorphous Silicon Films and Solar Cells

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A detailed investigation of the effects of prolonged postdeposition annealing on the performance of amorphous silicon (a-Si:H) solar cells and the properties of individual a-Si:H layers that are fabricated at low temperature of 120 °C is presented. A substantial improvement in all parameters of the current–voltage curves of these solar cells is observed upon annealing, consistent with an improvement in the collection voltage of the solar cells. Modifications of p-type layers during deposition of the solar cells are found to make no significant contribution to the annealing behavior of solar cells, while variations in the properties of n-type and intrinsic layers contribute substantially. The results indicate that the largest contribution to the annealing effect originates from changes in the electron $\mu\tau$ -product in the intrinsic absorber layer upon annealing, while changes in hole $\mu\tau$ -products have a minor contribution to the annealing effect in the solar cell. Besides a lack of significant changes in the number of recombination centers upon annealing, an improvement in the external quantum efficiency curves upon annealing may be accurately reproduced in computer simulations by assuming an increase in the band mobilities of both electrons and holes.

minimized. In the case of transparent polyethylene terephthalate (PET), which is frequently used as substrate for flexible photovoltaic devices, the process temperatures are limited to $T < 150^\circ\text{C}$,^[1] which reduces the electronic quality of the functional layers of the solar cell.^[2] In the present work, we investigate the effects of postdeposition thermal annealing on the performance of low-temperature amorphous silicon (a-Si:H) solar cells developed for flexible photovoltaics.^[3–5] Flexible solar cells attract interest in various applications, such as applications in building integrated photovoltaics, flexible and mobile power applications.^[6,7]

Thermal annealing processes may be used to improve the performance of various types of solar cells.^[8] In amorphous silicon solar cells, an improvement in photovoltaic performance could be observed upon post deposition annealing, especially when the layers are prepared at relatively

1. Introduction

Low deposition temperatures are essential for thin-film silicon solar cells prepared on cheap plastic substrates, allowing associated production costs of flexible solar cells and modules to be

low temperatures. For example, Brinza et al.^[5] have studied a-Si:H solar cells deposited at 100 °C and have observed that the efficiency could be substantially improved upon postdeposition annealing, mainly due to improvement in the open-circuit voltage. The work of Koch et al. concerned the properties of amorphous silicon solar cells deposited at 75 °C, a significant increase in photovoltaic efficiency upon annealing at temperatures of 110 °C, mainly due to improvement in the short-circuit current density.^[9] In the case of amorphous silicon germanium solar cells, Wang et al. observed an increase in the efficiency (up to 50% relative) for various annealing temperatures up to 230 °C.^[10] In general, an improvement in performance is related to the changes in the absorber layer upon annealing. Additionally, thermal annealing in amorphous silicon layers and solar cells will recover the electronic properties of a-Si:H layers and solar cell performance after prolonged illumination (known as Staebler–Wronski–Effect [SWE]^[11]) by annealing light-induced defects in the intrinsic absorber layer.

In contrast to the annealing of light-induced defects created by prolonged illumination, here we investigate the effects of long-term postdeposition annealing at a temperature of 120 °C on the performance of a-Si:H solar cells and individual layers, fabricated at low deposition temperatures ($T < 150^\circ\text{C}$). An improvement in all photovoltaic parameters deduced from the current–voltage (J – V) curves of a-Si:H solar cells is observed upon annealing (see Figure S1, Supporting Information), resulting in a significant efficiency improvement up to 34% relative, mainly caused by an

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increase in the fill factor (FF) by as much as 22% relative. In order to understand the origin of the observed effects, detailed studies of low-temperature silicon structures (layers and solar cells) are performed on glass substrates. We systematically investigate the annealing behavior of all functional layers in the device and establish a link between changes in the electronic properties of the functional layers and device performance upon annealing. For this purpose, the low-temperature silicon layers in the device are consecutively substituted by layers deposited at higher substrate temperature of 180 °C. These high-temperature layers are expected to be only weakly sensitive to postdeposition annealing at 120 °C, implying that the observed annealing effect in the solar cells may be linked to changes in the remaining low-temperature silicon layers.

In addition to the studies conducted on individual layers, solar cells having absorber layer materials with a wide range of electronic quality are evaluated, indicating that the magnitude of the annealing effect (e.g., the magnitude of FF increase upon annealing) is related to the electronic properties of the absorber layer in the as-deposited state. Optical characterization methods, such as variable intensity measurements (VIMs) and steady-state photo-carrier grating (SSPG) technique, are employed to understand the underlying physical mechanisms governing the observed annealing effects. Computer simulations using a simplified optical model are used to understand the changes in external quantum efficiency (EQE) curves upon annealing and relate the changes with carrier mobilities. The results of the present study are relevant for both fundamental understanding of the physical mechanisms responsible for the changes in the device performance upon annealing and for industrial development of low temperature both rigid or flexible thin-film silicon cells with improved efficiency.

2. Experimental Section

Hydrogenated amorphous silicon (a-Si:H) layers (individual and a-Si:H layers in solar cells) were fabricated by radio frequency plasma enhanced chemical vapor deposition (RF-PECVD) in a multichamber ultra high vacuum (UHV) deposition system

using a gas mixture of silane and hydrogen. The substrate temperature during deposition was either 120 °C or 180 °C. For intrinsic layers, silane concentration (SC) is defined as the ratio of silane flow $[\text{SiH}_4]$ to total gas flow $\text{SC} = \frac{[\text{SiH}_4]}{[\text{SiH}_4] + [\text{H}_2]}$ and was 16.7%, unless noted differently. Phosphine (PH_3 , 5% diluted in silane, 6 sccm flow) was added as doping gas for the deposition of n-type layers with a phosphorus concentration PC of 0.02 ($\text{PC} = \frac{[\text{PH}_3] \cdot 0.05}{[\text{SiH}_4]}$), with a total silane and hydrogen flow of 15 and 130 sccm, respectively. In the case of p-type layers, silane and hydrogen flows of 9 and 90 sccm were used, respectively, and trimethylborane $[\text{B}(\text{CH}_3)_3]$ diluted in He (2.54%) with a flow of 9 sccm was added as doping gas, resulting in a boron concentration (BC) of $\text{BC} = \frac{[\text{TMB}] \cdot 0.0254}{[\text{SiH}_4]} = 0.0254$. For the solar cells presented in Section 3.1 and 3.2 (except Figure 4), additionally methane was used with a flow of 5 sccm. More details on the deposition process can be found in the study by Wilken et al.^[12] Individual intrinsic a-Si:H layers having a thickness between 420 and 510 nm were prepared on Corning Eagle XG glass substrates. Solar cells in p-i-n deposition sequence were prepared on commercially available SnO_2 -coated glass substrates (Asahi-U type) with an absorber layer thickness around 450 nm. Evaporated silver pads were used as back contact, which define the cell area of 1 cm². Information on the fabrication of n-side illuminated solar cells can be found in the study by Wilken et al.^[13] Typical device structures for p- and n-side illuminated solar cells are shown in Figure 1a,b, respectively.

Annealing was conducted, for both solar cells and silicon layers, in dark conditions in ambient air and/or high vacuum ($\approx 10^{-6}$ mbar) at a temperature T_{ann} of 120 °C for up to 150 min in steps of 30 min.

Conductivities of individual layers were measured with evaporated coplanar silver contacts in vacuum. For measurements of photoconductivity σ_{ph} , as well as SSPG measurements, a He-Ne laser was used. Mobility-lifetime products of electrons $(\mu\tau)_e$ were evaluated from σ_{ph} using the following equation^[14]

$$\sigma_{\text{ph}} = eG(\mu\tau)_e \quad (1)$$

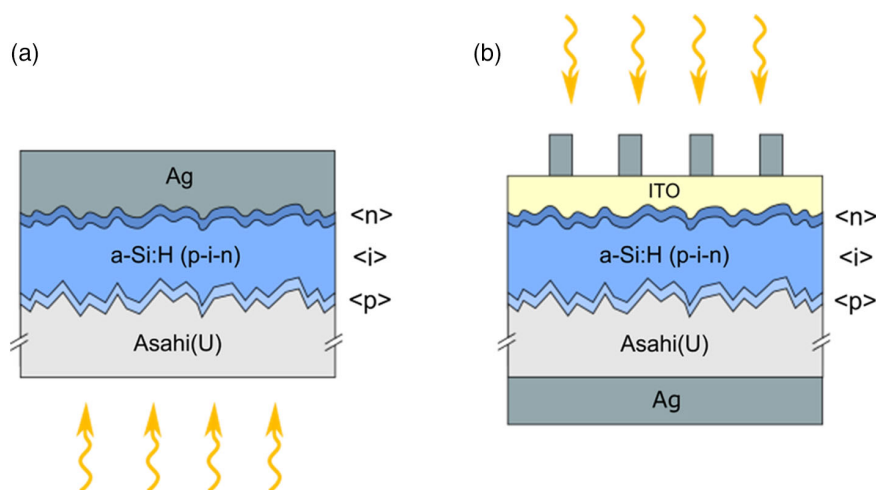


Figure 1. Schematic layer stack of an a-Si:H solar cell for the case of illumination through a) the p-type layer (p-side illuminated) and b) the n-type layer (n-side illuminated) where Ag layer at the bottom is used as an optical back reflector.

where e is the elementary charge. The generation rate G was calculated from photoconductivity, absorption coefficient, and thickness of each sample and was $1.7 \pm 0.3 \times 10^{18} \text{ cm}^{-3} \text{ s}^{-1}$.

In order to access the minority carrier (hole) transport properties, steady-state photocarrier grating technique was carried out on individual intrinsic layers. The sample structure was similar to that used for conductivity measurements, i.e., with evaporated coplanar silver contacts on top of the sample. SSPG measurements were performed for G values of $3.5 \pm 0.5 \times 10^{20} \text{ cm}^{-3} \text{ s}^{-1}$ with He–Ne laser with an applied DC bias in the ohmic and low electric field region, where electric field versus β was measured and found to be constant, indicating that only diffusion controlled transport dominates.^[15] The minority carrier hole diffusion lengths, L_D , was evaluated from the results of the measurement using the procedure described in the study by Günes et al.^[16] Mobility-lifetime products of holes $(\mu\tau)_h$ were evaluated from L_D using Equation (2)^[17]

$$L_D = \sqrt{2 \frac{e}{kT} (\mu\tau)_h} \quad (2)$$

where k is the Boltzmann constant and T is the absolute temperature. The measurements were performed at the Mugla Sıtkı Kocman University in Turkey and a detailed description of the measurement setup can be found in the study by Günes et al.^[16]

Optical absorption measurements by the constant photocurrent method (CPM)^[18] were used to estimate relative changes in the density of sub-bandgap defects.

Solar cells were characterized using a class A sun simulator for current density–voltage (J – V) measurements under 100 mW cm^{-2} AM1.5 illumination at a temperature of 25°C . FF, open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), and efficiency η were evaluated from these J – V curves. External quantum efficiencies were determined by measuring the differential spectral response of the solar cell.

VIMS^[19] were carried out to distinguish between the three main effects influencing the FF of a thin-film silicon solar cell: series resistance (R_s), shunt resistance (R_{sh}), and the collection of charge carriers. The latter was evaluated by the collection voltage (V_{coll}), defined by Equation (3)^[20]

$$V_{coll} = \frac{(\mu\tau)_{eff}}{\psi} \times E_{bi}^2 \quad (3)$$

with the effective mobility-lifetime product $(\mu\tau)_{eff}$ (see Shah et al.^[20] for a detailed explanation), the built-in field (E_{bi}), and a factor $1 < \psi < 2$, describing the deformation of the built-in field inside the intrinsic absorber layer.^[20] Current–density voltage curves were measured under various intensities of AM1.5 illumination by applying gray filters. The V_{coll} was evaluated by plotting the short-circuit resistance (R_{sc}), defined as the inverse slope of the J – V curve at $V = 0 \text{ V}$

$$R_{sc} = \left(\frac{dJ}{dV} \right)^{-1}_{V=0} \quad (4)$$

for each intensity level against J_{sc} .^[21] The R_{sh} was determined from the short-circuit resistance of J – V curves measured without illumination, where the photogenerated current is negligible

$$R_{sh} = R_{sc, \text{dark}} \quad (5)$$

The R_s was evaluated from the inverse slope of the J – V curve at $V = V_{oc}$ measured at 1 sun

$$R_{sc} = \left(\frac{dJ}{dV} \right)^{-1}_{V=V_{oc}} \quad (6)$$

It should be noted that both R_{sh} and R_s are given in $\Omega \text{ cm}^2$, consistent with the short-circuit current density used here (mA cm^{-2}) instead of current (mA).

Computer simulations were performed by wxAMPS software,^[22,23] which is an updated version of the popular simulation tool AMPS-1D (Analysis of Microelectronic and Photonic Structures). A layer stack in p–i–n configuration was built up in the simulator following the typical parameters for a-Si-based materials suggested in ref. [24], except for the bandgap (2.0 eV) and lower doping concentration ($8 \times 10^{17} \text{ cm}^{-3}$) for low-temperature deposited p-type a-Si:H layers. The basic optical model (without light trapping and TCO layers) was considered to keep the simulation simple and intuitive. The band mobilities μ_0 of electrons/holes in the intrinsic layer were varied from 1.0/0.10 to 1.4/0.14 to simulate the effect of the annealing process while keeping the ratio $\mu_{0,e}/\mu_{0,h} = 10$ constant. The calculated EQE curves were normalized to the EQE curve of the cell with the lowest mobilities (1.0/0.10) to show relative changes.

3. Results

3.1. Identifying Device Components Contributing to the Annealing Effect

The improvement in solar cell efficiency upon annealing, observed in the solar cells investigated here, can be a result of improved (photo)electrical properties in one or several functional layers and/or interfaces present in the device. The a-Si:H solar cell is a multilayer device consisting of a TCO layer, various types of silicon thin films, and a metal (Ag) layer (see also Figure 1). Therefore, a possible contribution from each particular layer to the observed annealing effect should be considered.

1) TCO layer. In the literature, improvement upon annealing of solar cells is sometimes related to changes in the TCO layer properties, particularly to a reduction in sheet resistance upon annealing.^[10] However, the Asahi-U substrates used here showed no evidence of change in the sheet resistance, even after prolonged annealing times of 20 h at 120°C . Accordingly, possible changes in the TCO layer upon annealing can be excluded as a reason for the improvement in cell performance upon annealing.

2) Metal back contact. Influence of the back contact on the annealing process, and particularly effects at the n-type a-Si: H/Ag interface, could be excluded, as similar improvements upon annealing were found in solar cells annealed before and after the metal back contact evaporation. Furthermore, the

annealing effect is similar for both Ag and ZnO:Al/Ag back contacts.

3) Amorphous silicon layers. The reasons above indicate that changes in the photovoltaic parameters of a-Si:H solar cells upon annealing are related to changes in the remaining layers: the amorphous silicon layers and/or interface properties that are the focus of the present work.

In order to analyze the contribution from each of the low-temperature silicon layers (p, i, and n types) to the observed improvement in solar cell performance upon postdeposition annealing, the low-temperature silicon layers in the device were consecutively substituted by layers deposited at higher substrate temperature of 180 °C. These high-temperature layers are expected to be only weakly sensitive to postdeposition annealing at 120 °C, implying that the observed annealing effect in the solar cells may be linked to changes in the remaining silicon layers deposited at low temperature. Due to the nature of designed experiments (e.g., an increase in the deposition temperature of some layers beyond the temperatures tolerable by PET substrates), the majority of experiments was performed on glass substrates.

The deposition temperatures of each layer in the investigated types of solar cells (A–D) are presented in Table 1 along with corresponding FF values in the as-deposited state.

The typical J – V parameters of the solar cell where the silicon layers are prepared entirely at 120 °C (sample A), together with changes in the J – V parameters upon annealing are shown in Table 2. It can be seen that the solar cell efficiency is improved by around 2% absolute (34% relative improvement) upon annealing within 120 min. The FF is the most influenced parameter upon annealing (relative improvement 22%), while the open-circuit voltage and short-circuit current density are improved less.

Apart from the variation in deposition temperature described above, the samples were prepared under similar deposition conditions. The electrical properties of a-Si:H layers usually improve when the substrate temperature is increased from 120 °C to temperatures in the range of 200 °C.^[2,12,25] Accordingly, the FF increases from solar cell A to sample D, when an increasing

number of a-Si:H layers is deposited at 180 °C instead of 120 °C. Information about the electrical and optical properties of the as-deposited silicon layers used in solar cells A–D can be found in Table S1, Supporting Information.

As the FF is the parameter most significantly improved upon annealing (see Figure S1, Supporting Information and related Table 2), changes in FF are focused upon below. In Figure 2, the improvement in FF upon annealing of the four types of a-Si:H solar cells is presented by plotting normalized FF values $FF_{\text{annealed}}/FF_{\text{as-deposited}}$ as a function of annealing time (t_{ann}).

Solar cell A, which was entirely fabricated at 120 °C (black squares), shows a significant increase in FF after 30 min of annealing, by up to 14.7% relative (corresponds to a $FF_{\text{annealed}}/FF_{\text{as-deposited}}$ value of 1.147 in Figure 2). The FF further improves with continued annealing, reaching a relative improvement of 20.3% after 120 min. Sample B, where only the p-type layer is deposited at higher T_s of 180 °C (blue triangles), shows a similar annealing characteristic, with the $FF_{\text{annealed}}/FF_{\text{as-deposited}}$ value of 22.9 % after 120 min annealing being only slightly higher than that of sample A, which may be considered to be within the error bar. This is a remarkable result, as the material properties of the p-type layer deposited at 180 °C differ significantly from that deposited at 120 °C (more than one order of magnitude difference in dark conductivity, see Table S1, Supporting Information), a fact that also leads to a considerable difference in absolute FF value in the as-deposited state (56.8–51.6%, see Table 1). In the case of sample C, where the p-type and the intrinsic layers are deposited at 180 °C (green diamonds), the improvement in FF upon annealing is considerably reduced, with the $FF_{\text{annealed}}/FF_{\text{as-deposited}}$ value being only 7.4% relative after 120 min annealing. For solar cell D, which was entirely fabricated at 180 °C (red circles), the effect of annealing at 120 °C on the FF is greatly diminished, with merely 1.2% relative improvement in the FF after 120 min annealing.

Table 1. Substrate temperatures (T_s) used for the deposition of p-type, intrinsic, and n-type a-Si:H layers in the solar cell samples. The absolute FF value (best efficiency p-side illuminated cells) in the as-deposited state $FF_{\text{as-deposited}}$ is shown for each sample.

Sample	$T_{s,p\text{-type}}$ [°C]	$T_{s,\text{intrinsic}}$ [°C]	$T_{s,n\text{-type}}$ [°C]	$FF_{\text{as-deposited}}$ [%]
A	120	120	120	51.6
B	180	120	120	56.8
C	180	180	120	66.0
D	180	180	180	72.2

Table 2. Typical J – V parameters of the solar cell (sample A) in the as deposited state (0 min annealing) and after 120 min annealing.

Annealing time [min]	H [%]	FF [%]	V_{oc} [mV]	J_{sc} [mA cm ^{−2}]
0	6.1	51.6	874	13.5
120	8.2	62.3	909	14.6

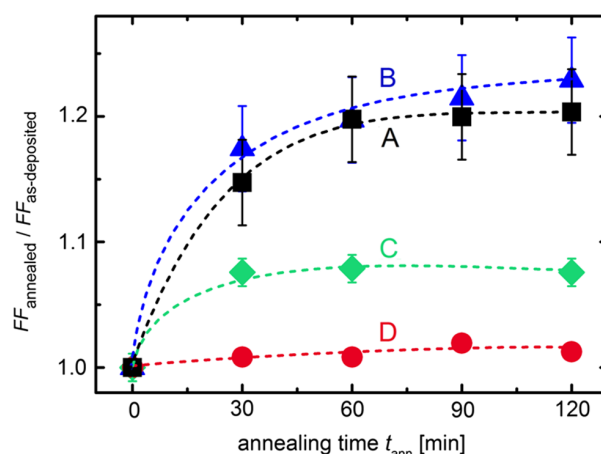


Figure 2. FF in the annealed state FF_{annealed} normalized to the as-deposited value $FF_{\text{as-deposited}}$ as function of postdeposition t_{ann} for the a-Si:H solar cells (p-side illuminated) A–D. The substrate temperatures used for the deposition of each layer in the four types of samples are presented in Table 1 along with absolute FF values in the as-deposited state. Lines are guides to the eye. The error bars are calculated based on the measurements of three solar cells in each state.

3.2. Differentiating Contributions to the FF Improvement upon Annealing

The FF of an a-Si:H solar cell in p-i-n configuration may be influenced by various parameters, such as the series (R_s) and shunt (R_{sh}) resistance of the device, as well as the collection efficiency of generated charge carriers.^[26] In order to distinguish between these three effects, VIMs^[15] were carried out for various annealing times on a-Si:H solar cells deposited entirely at 120 °C and entirely at 180 °C, which show the strongest and weakest annealing effect, respectively. The cell prepared at 120 °C with slightly lower initial FF was selected in order to observe stronger differences between two studied cases. The resulting values of R_s , V_{coll} , and R_{sh} are plotted against annealing time in **Figure 3b–d**, respectively, along with FF values in **Figure 3a**.

For the low-temperature solar cell (black squares in **Figure 3**), the FF increases significantly from 41.9 % in the as-deposited state to 50.9% after 120 min annealing at 120 °C. Simultaneously, the series resistance of the device R_s is reduced from 40.3 to 33.7 $\Omega \text{ cm}^2$. The collection voltage follows the trend of the FF, increasing considerably by a factor of more than 2: from 6.5 V in the as-deposited state to 14.6 V after 120 min annealing. The shunt resistance shown in (d), on the other hand,

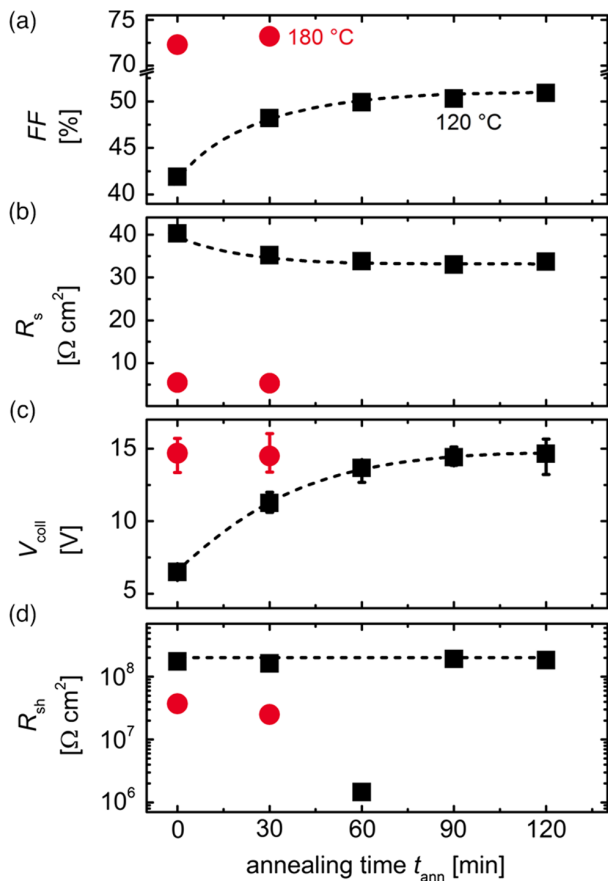


Figure 3. a) FF, b) R_s , c) V_{coll} , and d) R_{sh} of an a-Si:H solar cell (p-side illuminated) deposited at 120 °C as function of t_{ann} (black squares). The values for an a-Si:H solar cell deposited at 180 °C are shown for comparison (red circles). Lines are guides to the eye.

shows no influence of the postdeposition annealing in the investigated range, being constant at $R_{sh} = (1.78 \pm 0.15) \times 10^8 \Omega \text{ cm}^2$ (given that the data point at $t_{ann} = 60$ min is regarded as outlier). The solar cell deposited at 180 °C (red circles), on the other hand, shows only a slight change upon annealing at 120 °C in the investigated parameter range. As the collection voltage is similar to that of the low-temperature solar cell in the annealed state and the shunt resistance is even a bit lower compared to the low-temperature device, it can be concluded that the higher FF of 73.2% after 30 min annealing for this solar cell can be related to the significantly lower series resistance of $R_s = 5.4 \pm 0.1 \Omega \text{ cm}^2$ in the device.

Correlation between material quality of the a-Si:H absorber layer and FF of the solar cells was investigated for various types of a-Si:H solar cells, including flexible solar cells prepared on PET substrates. In **Figure 4**, the improvement in FF upon annealing (expressed as normalized FF $FF_{150min}/FF_{as-deposited}$ after 150 min annealing time) for various types of a-Si:H solar cells is plotted as a function of photoresponse of the intrinsic absorber implemented in the solar cell. Note that the photoresponse is evaluated on individual layers, where the electronic transport is measured perpendicular to the film growth direction, while in the case of the solar cells the electronic transport in the growth direction takes place. It is generally believed that the amorphous silicon may be considered as an isotropic material, and the isotropic electronic transport properties are observed.^[27] In the case of solar cells, additional effects, such as p/i and n/i interface recombination processes, may contribute to the carrier collection in the device. The annealing time of 150 min used for the samples presented in **Figure 4** is due to stronger effect observed in solar cells prepared on PET substrates. The photoresponse, defined as the ratio of photo to dark conductivities, serves as a measure for the material quality and is greatly influenced by the $\mu\tau$ -product of charge carriers. The photoresponse of the intrinsic layer was varied by adjusting the SC during deposition between 4.2% and 16.7% (black squares), varying its substrate

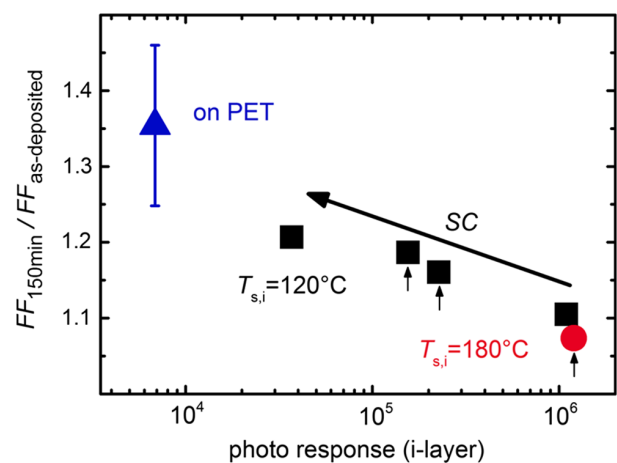


Figure 4. FF after 150 min annealing time FF_{150min} normalized to the as-deposited value $FF_{as-deposited}$ of a-Si:H solar cells (p-side illuminated) deposited at various SC of the intrinsic absorber layer as function its photoresponse (black squares). Solar cells/layers on PET (blue triangle) and deposited at 180 °C (red circle) are shown for comparison. The small arrows indicate the layers analyzed in more detail in the Section 3.3.

temperature $T_{s,i}$ (red circle), as well as changing the substrate from glass to PET (blue triangle). It should be considered here that in the latter two cases not only the conditions for i-layer deposition were changed, but also the p-type and n-type layers were deposited at 180 °C and on PET substrate, respectively. Note that the photoresponse of the layer prepared on PET is below 10^4 , which could possibly be related to the changes in the material properties compared to the layers on glass substrate. It is known that the thin film growth may be substrate dependent. For example, in contrast to rigid glass substrates, the flexible PET substrate may have different thermal coupling during the deposition process, which may change the properties of plasma during PECVD process as well as the properties of the grown materials.

A trend of reduced improvement in FF upon annealing with improving material quality (=enhanced photoresponse) of the intrinsic a-Si:H absorber layer can be observed. The link between changes in the mobility-lifetime products and cell performance upon annealing is more closely investigated in Section 3.3. Three samples, indicated by small arrows in Figure 4, were selected for this investigation.

3.3. Effect of Annealing on Mobility-Lifetime Products in Intrinsic a-Si:H

In order to better understand the relation between mobility-lifetime products in the absorber layer and FF of the solar cell upon annealing, three types of intrinsic a-Si:H layers were chosen for closer investigation. The deposition conditions of these samples as well as resulting FF values, when implemented in a solar cell, are presented in Table 3.

Mobility-lifetime products of electrons and holes were evaluated from the results of measurements of photoconductivity and SSPG on individual layers, respectively, and are shown in Figure 5.

In the case of sample 120_16.7 (black squares), which exhibits the strongest improvement in FF upon annealing when implemented in a solar cell (see Table 3), a large improvement in the electron mobility-lifetime product $(\mu\tau)_e$ due to postdeposition annealing is observed, namely, nearly one order of magnitude from $2.0 \times 10^{-8} \text{ cm}^2 \text{ V}^{-1}$ in the as-deposited state up to $1.3 \times 10^{-7} \text{ cm}^2 \text{ V}^{-1}$ after 120 min annealing. The mobility-lifetime product $(\mu\tau)_h$ of holes simultaneously increases by a factor of 1.5 from $1.4 \times 10^{-9} \text{ cm}^2 \text{ V}^{-1}$ to $2.1 \times 10^{-9} \text{ cm}^2 \text{ V}^{-1}$. Sample 120_12.5 (green triangles), which was prepared with a

lower silane concentration compared to sample 120_16.7, shows higher values for $\mu\tau$ -products of both electrons and holes in the as-deposited state, namely, $6.7 \times 10^{-8} \text{ cm}^2 \text{ V}^{-1}$ and $5.2 \times 10^{-9} \text{ cm}^2 \text{ V}^{-1}$ for $(\mu\tau)_e$ and $(\mu\tau)_h$, respectively. In the case of $(\mu\tau)_e$, the effect of annealing is lower compared to sample 120_16.7, so that after 120 min annealing time values are similar for both types of layers. The improvement in $(\mu\tau)_h$ upon annealing, on the other hand, is only slight by 5.7% up to $5.5 \times 10^{-9} \text{ cm}^2 \text{ V}^{-1}$. The sample deposited at high temperature (180_16.7) shows the highest values for mobility-lifetime products in the as-deposited state. As expected, the $\mu\tau$ -products are hardly affected by annealing at 120 °C, with no change visible in $(\mu\tau)_h$ after 120 min annealing and only slight improvement in $(\mu\tau)_e$ (from 1.7 to $2.4 \times 10^{-7} \text{ cm}^2 \text{ V}^{-1}$).

Implementing the layers presented in Table 3 in a-Si:H solar cells (using p- and n-type a-Si:H layers deposited at 120 °C under nominally identical deposition conditions), the differences in the device performance may be linked to the differences in the properties of individual intrinsic a-Si:H layers. In Figure 6, the FF values of these solar cells are plotted against the corresponding $\mu\tau$ -product in intrinsic amorphous silicon, measured on individual layers. The FF is presented as a function of (a) the $(\mu\tau)_e$ -product and (b) the $(\mu\tau)_h$ -product of the implemented intrinsic a-Si:H layer. The data comprise the values of layers and solar cells for various annealing times (0, 30, 60, and 120 min) and the three types of layers investigated (see Table 3).

A correlation can be found between the FF in the solar cell and $(\mu\tau)_e$ for the individual samples as well as over entire range of deposition conditions of the intrinsic layer and annealing times, indicating that an improvement in the $(\mu\tau)_e$ leads to an improvement in FF values. On the other hand, no comprehensive relation is found for the three types of layers with respect to the hole $\mu\tau$ -product (for each particular sample, an improvement in the FF has a weak relation with hole $\mu\tau$ -product which is schematically shown by the guidelines in (b)). These results suggest that in the investigated type of a-Si:H solar cell, electrons are likely the carrier type limiting the device performance. The observed improvement in $(\mu\tau)_e$ upon annealing would then lead to the observed improvement in FF and thus efficiency of the solar cell. In the next section, possible reasons of improvement of the $(\mu\tau)_e$ -product upon annealing will be evaluated.

3.4. $(\mu\tau)_e$ Improvement upon Annealing

Bearing in mind indications that transport properties ($\mu\tau$ -products) of the charge carriers are enhanced upon annealing, it needs now to be considered if this enhancement is due to an increased 1) lifetime and/or 2) mobility of the charge carriers. In fact, both $(\mu\tau)_e$ and $(\mu\tau)_h$ increase upon annealing in the case of sample 120_16.7, indicating that the improved $(\mu\tau)_e$ -product is likely not due to a shift in the Fermi level, as pointed out by Brüggemann and Morgado.^[17,28] In addition, the improvement of both $(\mu\tau)_e$ and $(\mu\tau)_h$ suggests that the annealing effect is unlikely to be the result of incoming contaminations during the annealing process in air or diffusion of dopants within the layer stack. Another possible scenario is the effect of changing defect densities (related to carrier lifetime) and/or mobilities. In the following, sample 120_16.7, showing the strongest

Table 3. Overview of investigated intrinsic a-Si:H layer samples deposited at substrate temperatures $T_{s,i}$ and at silane concentrations SC_i . The absolute FF value $FF_{\text{as-deposited}}$ and the FF improvement $FF_{120\text{min}}/FF_{\text{as-deposited}}$ after 120 min annealing at 120 °C, when implemented in a solar cell, are shown for each sample. A-Si:H p- and n-type layers in the solar cells were deposited at 120 °C in all cases under nominally identical deposition conditions. Sample code denotes deposition temperature and SC of respective layers.

Sample	$T_{s,i}$ [°C]	SC_i [%]	$FF_{\text{as-deposited}}$	$FF_{120\text{min}}/FF_{\text{as-deposited}}$
120_16.7	120	16.7	55.8	1.183
120_12.5	120	12.5	59.2	1.155
180_16.7	180	16.7	64.6	1.103

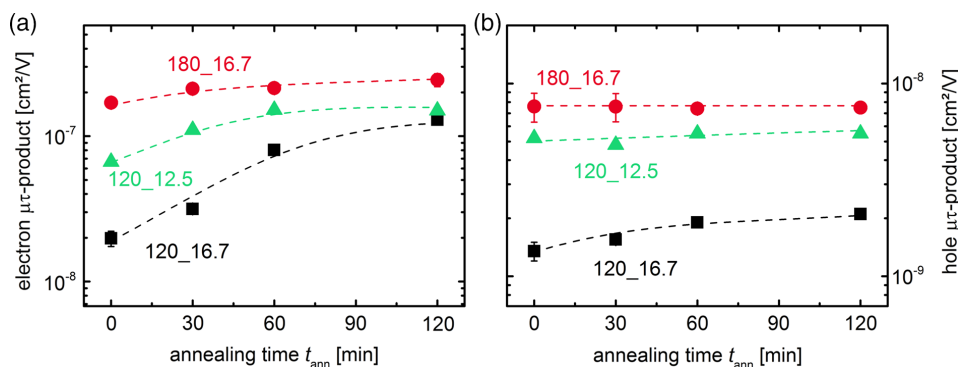


Figure 5. Mobility-lifetime ($\mu\tau$) products of a) electrons, as determined from measurements of photoconductivity and of b) holes, as determined from the results of SSPG measurements, for three types of intrinsic a-Si:H absorber layers deposited under different substrate temperatures T_s and silane concentrations SC (see Table 2 for explanation). Lines are guides to the eye.

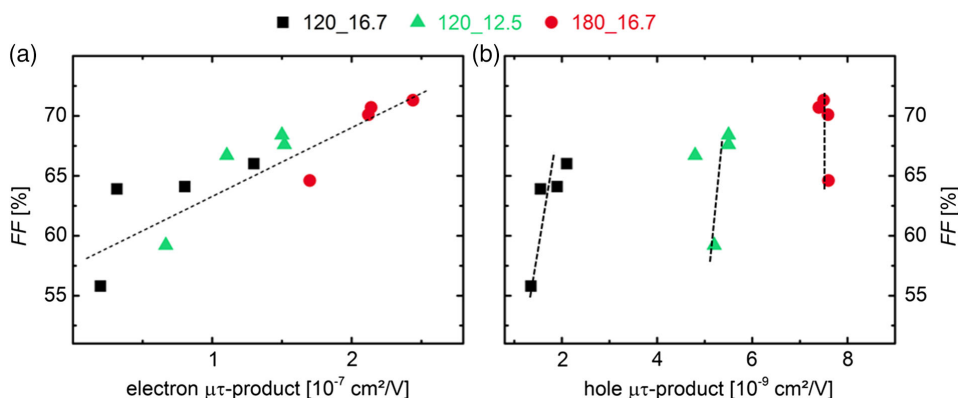


Figure 6. FF of a-Si:H solar cells (p-side illuminated) in various annealed states (0, 30, 60, and 120 min) as a function of a) $(\mu\tau)_e$ -product of electrons and b) $(\mu\tau)_h$ -product of holes in the respective implemented intrinsic a-Si:H layer. The applied intrinsic layers are samples 120_16.7 (black squares), 120_12.5 (green triangles), and 180_16.7 (red circles) (see Table 3). The lines are a guide to the eye.

increase in $(\mu\tau)_e$ upon annealing, was selected for more detailed investigation. Subgap absorption spectra are evaluated in Section 3.4.1 in order to investigate possible changes in the defect density, which may in turn result in changes of charge carrier lifetimes. In Section 3.4.2, a possible change in mobility of the charge carriers is evaluated by performing computer simulations using wxAMPS software.

3.4.1. Defect Density Evaluated by CPM

The defect density may be estimated by measurements of subgap absorption via CPM.^[18,29,30] Absorption spectra measured by CPM are shown in **Figure 7** for sample 120_16.7 (which shows the strongest annealing effect) in the as-deposited state and after 60 min annealing time.

From these measurements, no change in subgap absorption can be detected after 60 min annealing at 120 °C, which indicates that the number of recombination centers in the intrinsic absorber layer does not change upon annealing. In order to estimate if observed changes in the $(\mu\tau)_e$ -product are expected to show up in subgap absorption measurements, we conduct the following simple calculations. The subgap absorption $\alpha_{1.2 \text{ eV}}$

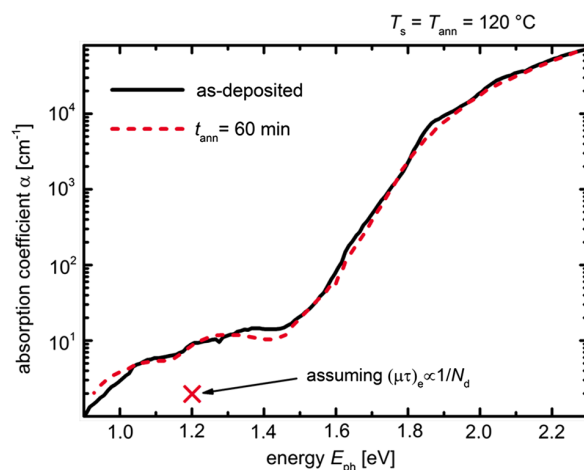


Figure 7. Absorption spectra measured by CPM on sample 120_16.7 in the as-deposited state (black solid line) as well as after 60 min annealing at 120 °C (red dashed line). The red cross indicates the expected value of absorption coefficient (at 1.2 eV) after 60 min annealing assuming that the increase in $\mu\tau$ -product is due to an increased lifetime of electrons and that the $(\mu\tau)_e$ is inversely proportional to the defect density N_d .

may be correlated to the defect density in a-Si:H films using a calibration factor.^[18] We use 3×10^{16} in this case. Assuming that the improvement in $(\mu\tau)_e$ is solely caused by an increase in τ_e , and that $(\mu\tau)_e \propto 1/N_d$,^[14] one can calculate the expected N_d after 60 min annealing based on the $(\mu\tau)_e$ value in Figure 5a. The corresponding subgap absorption $\alpha_{1.2\text{ eV}}$ after 60 min annealing is indicated by a red cross in Figure 7, and is substantially below the error bar of the measurement, suggesting that the improvement in $(\mu\tau)_e$ and thus charge carrier collection and FF is unlikely due to a reduction in deep defect density.

3.4.2. Mobility

As the results in Section 3.4.1 indicate that the increased $(\mu\tau)_e$ is not caused by a reduction of the deep defect density and thus the active recombination centers in the intrinsic absorber layer, possible changes in the mobility of charge carriers are investigated. Band mobilities describe the transport of free charge carrier in the extended states (i.e., conduction band in the case of electrons and valence band in the case of holes), while the drift mobility considers the time charge carriers spent trapped in the band tails states until they are re-excited into the extended states. According to Street,^[14] the drift mobility μ_D is decisive for the device performance of an a-Si:H solar cell and is given by

$$\mu_D = \frac{\mu_0}{1 + f_{\text{trap}}} \quad (7)$$

where μ_0 corresponds to the free carrier (band) mobility in the extended states and f_{trap} is the ratio between the time a carrier spends in localized traps in the band tail and the time it spends in the extended states. Band mobilities cannot unambiguously be accessed experimentally as all measurement techniques, such as the time-of-flight method for example, measure the average motion of carriers over a longer time, thus trapping events are included.^[14] Furthermore, the transport conditions in a solar cell under a high constant generation rate cannot be compared directly with the conditions prevailing in the time-of-flight experiment.

In order to investigate if a change in charge carrier mobility in the absorber layer may be related to improvements in the photovoltaic device upon annealing, computer simulations using

wxAMPS software^[22,23] were carried out. In our previous work,^[13] changes in EQE for p-side as well as n-side illuminated solar cells were investigated in order to get information on changes in charge carrier collection of electrons and holes. **Figure 8** shows the experimental EQE curves of the p-side as well as n-side illuminated solar cell from Wilken et al.^[13] in the annealed state normalized to the as-deposited state for various annealing times (30, 60, and 120 min). EQE curves have been simulated for various values of band mobilities μ_e and μ_h ($1.0 < \mu_e < 1.4$ and $0.10 < \mu_h < 0.14$). Band mobilities varied here would simultaneously influence the drift mobility, according to Equation (7). A similar approach was followed in the study by Reynolds et al.,^[31] who studied solar absorbers deposited either side of the transition from amorphous to microcrystalline growth. The target in that work was also to match the EQE curve behavior by varying carrier mobility. The simulated EQE curves in **Figure 9** were normalized to the EQE curve for a solar cell with $\mu_e = 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $\mu_h = 0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (nominally corresponding to as-deposited state values) in the intrinsic absorber layer.

Though a simplified model (no glass/TCO substrate, no light trapping) was used, comparison of Figure 8 and 9 shows that the improvement in experimental EQE curves may qualitatively be reproduced by increasing the band mobility of electrons and holes (μ_e and μ_h , respectively). The general trends are similar for simulation and experiment, i.e., a pronounced minimum in EQE improvement ratio between 500 and 600 nm (compare Figure 8a with Figure 9a) and an increased improvement ratio in the short wavelength range for the n-side illuminated solar cell (compare Figure 8b with Figure 9b). The differences to the experimental results in the range $\lambda < 350 \text{ nm}$ result from the missing glass/TCO substrate in the simulation, which leads to parasitic absorption and thus diminished EQE improvement in the case of experimental results. The approach used in our simulations replicates well experimentally observed changes in J–V characteristics (see Figure S2, Supporting Information): the major experimentally observed trends, such as changes in FF and J_{sc} could be well reproduced. Due to the simplified model used, the values of V_{oc} are overestimated and are limited by the properties of the doped layers (see, e.g., Wang et al.^[32] addressing limiting factors defining open-circuit voltage) and not by the changes in the i-layer properties over the investigated range of mobilities. Note that the parameters of doped layers were not

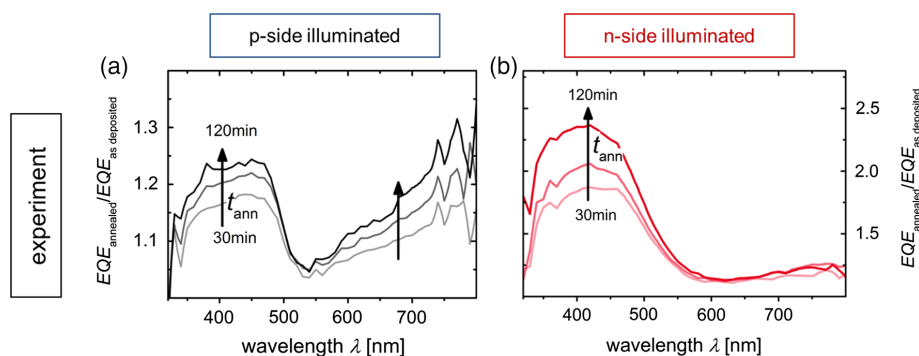


Figure 8. Experimental $\text{EQE}_{\text{annealed}}$ curves in various annealed states (30, 60, and 120 min) normalized to the $\text{EQE}_{\text{as-deposited}}$ curve in the as-deposited state of a) a p-side and b) an n-side illuminated a-Si:H solar cell.

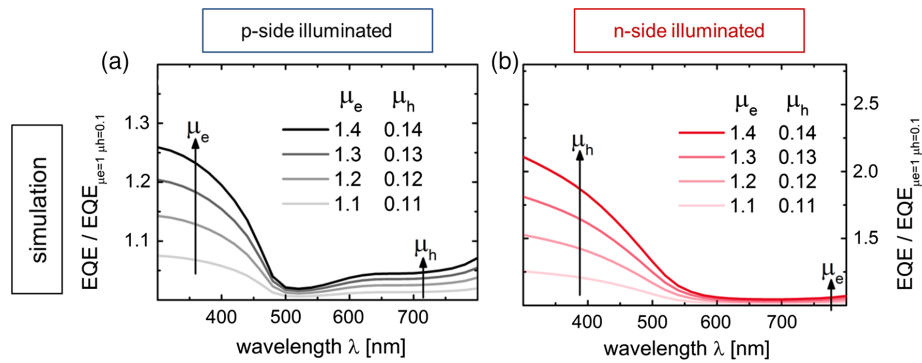


Figure 9. Simulated EQE curves normalized to the EQE curve for $\mu_e = 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $\mu_h = 0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for various values of μ_e and μ_h of a) a p-side and b) an n-side illuminated a-Si:H solar cell. The ratio $\mu_e/\mu_h = 10$ is kept constant.

changed in simulations, while changes in the doped layer properties may contribute to the changes in V_{oc} upon annealing. Overall, the results of simulations support well the views that mobility changes upon annealing play a major role in the improvement of solar cell performance. More sophisticated simulation models may be needed in the future to address the changes V_{oc} in upon annealing, which is not the main focus of the present work.

4. Discussion

Assuming that a change in, e.g., dark conductivity of the low temperature p-type layer would govern an improvement in solar cell performance upon annealing (due to, e.g., an improvement in the built-in field of the device), one would expect varying annealing characteristics for solar cells using p-type layers with different material properties in the as-deposited state. The magnitude of the FF improvement of samples A (120 °C p-type layer) and B (180 °C p-type layer) in Figure 2 therefore suggest that the low-temperature p-type layer investigated here has only minor contribution to the annealing effect in this type of solar cell. The insensitivity of the p-type layers studied here to postdeposition annealing may partially be explained by the fact that the p-type layer is already subjected to an annealing treatment during solar cell deposition (during subsequent intrinsic and n-type layers deposition).

Supposing that the high-temperature (180 °C) layers are not sensitive to postdeposition annealing at 120 °C, the FF improvement upon annealing in the cases of samples A and B can be related to changes in the low-temperature intrinsic and n-type a-Si:H layers. For sample C, only the n-type layer is deposited at low temperature of 120 °C, thereby the remaining improvement in FF of 7.4 % after 120 min annealing time may be related to changes in this layer. This is supported by comparison of samples C and D (green diamonds and red circles in Figure 2), where the improvement in FF upon annealing at 120 °C almost vanishes (down to 1.2% after 120 min annealing) due to the increased deposition temperature of the n-type layer. In conclusion, the results suggest that the largest contribution to the annealing effect is due to changes in the intrinsic a-Si:H absorber layer (reduction of the FF improvement upon annealing from

22.9% to 7.4%, compare blue triangles and green diamonds in Figure 2). Though from these results no unambiguous conclusions can be drawn to distinguish between bulk and interface annealing effects, e.g., if it is a bulk effect in the intrinsic absorber layer and/or an interface effect at the p(180)/i(120) interface, whose quality may also be affected by changes in the substrate temperature of the intrinsic a-Si:H layer.

Based on the results shown in Figure 3, the reduction of ohmic shunts in the device structure seems unlikely to be the reason for the improvement in FF upon annealing because R_{sh} hardly changes in the investigated range of annealing time. The increase in FF can consequently be ascribed to a significant increase in charge carrier collection, as measured by V_{coll} , as well as a reduced series resistance in the device. The reduction in series resistance may be related to a possible conductivity increase in the intrinsic absorber and/or doped layers, as indicated by an increasing dark conductivity of the p- and n-type a-Si:H layers (see Wilken et al.^[13]). However, the results presented in Section 3.1 indicate that the conductivity in the p-type layer has only minor influence on the annealing behavior.

The considerable increase in V_{coll} suggests a significant increase in charge carrier collection efficiency in the device upon postdeposition annealing. Previous results also found an improvement in charge carrier collection by investigating external quantum efficiencies of various types of a-Si:H solar cells as a function of annealing time.^[13] According to Equation (3), possible reasons for an improvement in V_{coll} and thus charge carrier collection may be related to several aspects discussed below, namely, 1) increase in the built-in field, 2) changes in the built-in field distribution, and 3) increase in $\mu\tau_{eff}$ of charge carriers in the intrinsic absorber layer.

1) Increase in the $E_{bi} = V_{bi}/d$, where V_{bi} is the built-in voltage in the device and d is the thickness of the intrinsic absorber layer. As no variation in the thickness of the amorphous silicon layers could be detected upon annealing (not shown), an increasing built-in field may be linked to a rise in built-in voltage. The built-in voltage is mainly determined by the Fermi-level positions and thus activation energies in the p- and n-type a-Si:H layers.^[32] The observed increase in dark conductivity in the study by Merten et al.^[19] would therefore imply an increase in E_{bi} , though, again, the results in Section 3.1 suggest that a change in dark conductivity of the p-type layer has no significant influence on

the annealing behavior. A possible explanation may suggest that the p-type layer activation energy is not the limiting quantity for the built-in voltage, but changes in the n-type layer (activation energy) take place upon annealing. The increase in dark conductivity of the n-type layer after 120 min annealing presented in the study by Wilken et al.^[13] corresponds to a reduced activation energy by 0.03 eV, which fits well to the observed increase in open-circuit voltage of 0.03 V upon annealing in Wilken et al.^[13] The contribution from the n-type layer would also explain the remaining improvement in FF upon annealing, when only the n-type layer is deposited at low temperature (cell C in Figure 2).

2) Furthermore, the distribution of the built-in field within the intrinsic absorber layer may change upon annealing. This is expressed by the ψ -value in Equation (3). Charged defects or ionized contaminations in the intrinsic absorber layer may change the charge distribution and thus deform the electrical field, hindering charge carrier extraction.^[33]

3) Increase in $(\mu\tau)_{\text{eff}}$, implying increasing mobilities and/or lifetimes of charge carriers in the intrinsic a-Si:H absorber layer upon annealing.

Overall, the results of VIM indicate that besides a reduction in series resistance, the charge carrier collection efficiency is greatly enhanced upon postdeposition annealing. Possible processes in the device include an enhanced built-in field by an increased built-in voltage (resulting from an increased dark conductivity of the n-type layer) and/or reduced number of recombination centers (electronic defects/contaminations) in the bulk intrinsic layer, as well as increased $\mu\tau$ -product of charge carriers in the intrinsic layer.

A reduction in silane concentration during film deposition can improve the material quality of a-Si:H thin films deposited at low temperatures, as previously observed.^[2,34] As visible from Figure 4 and 5, the mobility-lifetime products of both electrons and holes in the as-deposited state and thus the photoresponse in the intrinsic a-Si:H layer are improved by this measure (compare samples 120_16.7 and 120_12.5). This entails a reduction in the annealing effect on the $\mu\tau$ -product for sample 120_12.5. However, the annealing effect, when these layers are implemented in the solar cells, is still quite large with up to 16 % relative increase in the FF after 120 min (see Table 3). Considering that the $\mu\tau$ -product of holes is hardly improving upon annealing, this suggests that the changes in hole transport properties have minor contribution to the annealing effect in the solar cell. In general, it is a subject of discussion if the device performance is governed by electron and/or hole transport.^[35–37] It was suggested that the charge carrier collection and thus device performance is limited by a given carrier type (electrons or holes) and only an improvement in the $\mu\tau$ -product of the limiting carrier type will improve the solar cell performance.^[36] In the case of uniformly absorbed light, Hack and Shur have shown that hole transport will mainly determine the device performance in an a-Si:H solar cell, as its $(\mu\tau)_h$ -product is considerably smaller.^[36] In the case of AM1.5 illumination however, light is mainly absorbed in the front part of the solar cell. For the case of n-side illuminated solar cells (see Figure 1b), this means that the majority of charge carriers are generated near the n-type layer. Accordingly, holes have to travel through the entire absorber layer to be collected at the p-type contact, and will thus be the limiting charge

carrier.^[36,38] For p-side illuminated solar cells, the situation is more complex. Here, the device performance is governed by a trade-off between slow holes that have to travel a shorter distance toward the p-type layer, and faster electrons traveling a longer distance toward the n-type layer. As a result, it cannot easily be concluded which charge carrier type is limiting the carrier collection and thus V_{coll} and FF of p-side illuminated solar cells. By correlating solar cell performance (i.e., FF) upon annealing to $\mu\tau$ -products of both electrons and holes in the intrinsic a-Si:H layers (Figure 6), one can suggest that the $(\mu\tau)_e$ -product is limiting the solar cell performance in the investigated type of a-Si:H solar cell.

The results of simplified computer modeling show that the improvement in EQE upon annealing may well be reproduced by increasing the band mobilities of both electrons and holes. In the photovoltaic device, the decisive drift mobility may not only be improved by increased band mobility, but also by a reduced time that a carrier spends trapped in the band tails states (cf., Equation (6)). The enhanced $(\mu\tau)_e$ -product of electrons in the intrinsic a-Si:H layer might thus be caused by, for example, a steepening of the conduction band tail and a corresponding reduction in the number of localized states in this band tail upon annealing. Since the band tail absorption in the range $1.5 \text{ eV} < E_{\text{ph}} < 1.8 \text{ eV}$ is governed by the shape of the broader valence band tail in amorphous silicon, a change in the slope of the conduction band tail would not be visible (see Figure 7).

5. Conclusion

In the present work, the effects of prolonged postdeposition annealing at a temperature of 120 °C on the properties of low-temperature amorphous silicon individual layers and the performance of solar cells were systematically investigated. Comparison of changes in the properties of individual layers and solar cells upon annealing indicates that the major contribution to the improvement in the solar cell performance originates from changes in the intrinsic and also n-type layers, while p-type layers investigated here have only minor contribution to the improvement in FF upon annealing. The largest contribution to the annealing effect was related to changes in the intrinsic absorber layer, accompanied by a significant improvement in the collection voltage. Possible processes responsible for the improvement in device performance upon annealing were discussed, including 1) an improvement in the built-in field in the solar cell, related to an increased built-in voltage due to an increased dark conductivity of the n-type layer, 2) changes in the number of electronic defects/recombination centers in the bulk intrinsic layer, and 3) increased $\mu\tau$ -product of charge carriers in the intrinsic layer. Our results suggest that the main contribution to the annealing effect results from changes in $\mu\tau$ -products of charge carriers in the intrinsic absorber layer upon annealing. Moreover, separate evaluation of changes in both electron and hole transport properties upon annealing by steady-state photoconductivity and photocarrier grating methods, respectively, indicates that the changes in the hole $\mu\tau$ -product of the intrinsic absorber layer have minor contribution to the annealing effect in the solar cell, suggesting that the majority carrier (electron) transport properties limit the device performance. Correspondingly, an improvement in $(\mu\tau)_e$ results in the

improvement in the solar cell performance upon annealing. Interestingly, absorption spectra measured on individual intrinsic a-Si:H layers by the CPM indicate no significant changes in the number of recombination centers upon annealing, suggesting that the improvement in $(\mu\tau)_e$ and thus charge carrier collection and FF in these a-Si:H solar cells is unlikely due to a reduction in the density of recombination centers. In turn, the improvement in EQE upon annealing may be well reproduced in simplified computer modeling assuming an increase in the band mobilities of both electrons and holes.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

flexible solar cells, photovoltaics, silicon, thin films

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